# UDK3 Transfer Protocol

The CESYS Unified Development Kit 3 offers communication channels between a host PC and IP cores in FPGAs of CESYS boards and modules. Different kinds of physical channels are supported. At the time of writing in February 2014, USB 3.0 is available - Ethernet is planned.

The API function calls for reading from and writing to IP cores are address based. Most target designs are also address based (Typically Wishbone or AXI4) but the channels between the PC and the target design are serial data streams.

The UDK3 transfer protocol describes a data structure to convert address based accesses into stream data and vice versa.

It is also possible to embed multiple streams together with address based accesses in the UDK3 transfer protocol. In this case, the streams are treated as address based transactions with a fixed address (no auto-increment) and bursting enabled.

# Data path architecture

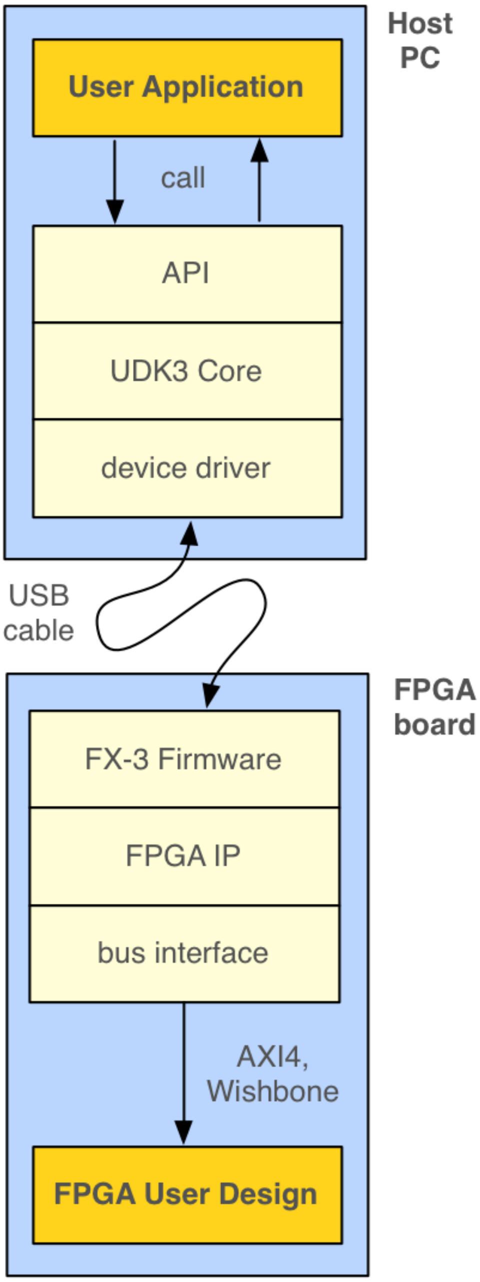
UDK3 Data path architecture is similar for all supported physical interfaces. The API functions, methods and classes are the same for different FPGA boards and Host Operating systems. Interchangeable APIs for different programming languages are available.

The supported languages are C, C++, .NET, Java and Python.

In the users FPGA design, API calls of the users application manifest as read and write bus-cycles. Everything between the API call and the bus-cycle is handled by the UDK3. Although it does not hinder, users are not forced to have knowledge about the details of the data channel (i.e. USB 3.0 or Ethernet) to use the UDK3 in their projects.

The UDK3 transfer protocol has support for burst mode and constant-address. Bursting raises the effective data transfer rate, mainly when accessing external memory through burst-capable memory controllers. In AXI4-based SoC designs, bursting is very common and supported by most Xilinx IPs. Constant address, however, is something that would map best to a AXI4STREAM interface.

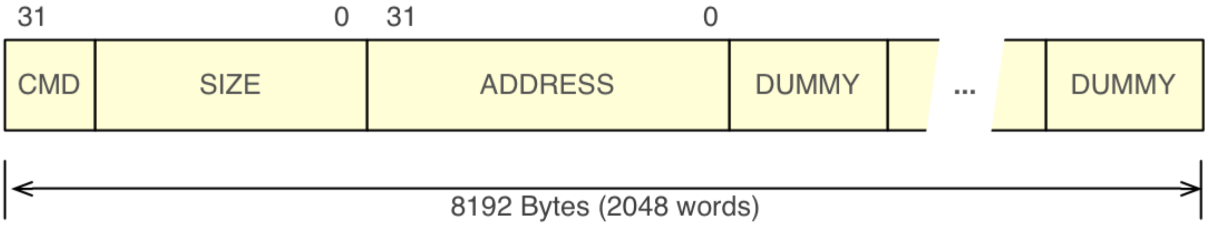
Not all reference designs make use of all available features. The reference design for the Wishbone bus (efm02_soc) implements constant address but not bursting. It is still able to keep up with the USB 3.0 data rates. The upcoming AXI4 reference design (in development) will support bursting, but initially not constant address.



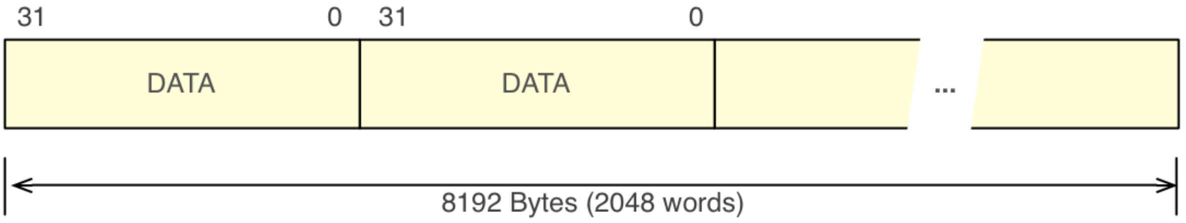
# Data Structure

The following description of the data structure is for information only. It is used internally to serialize the address-based transfers. It can be treated as a black box when using the UDK3 in own designs. The data structure of the Cesys UDK3 is similar to the structure of the previous UDK but the block length was increased from 1k to 8k for USB 3.0 devices and  for USB 3.0 devices that fell down to USB 2.0 because the host adapter does not support USB 3.0.

On response to an API call, the Host sends:



Then Host or Device sends (depending on transfer direction bit):



CMD and SIZE

bit 31: transfer direction.

1 = H2P (Host to Peripheral)

0 = P2H (Peripheral to Host)

bit 30: address mode

1 = auto increment address (API default).

0 = constant address.

bit 29: burst

1 = enable bursting.

0 = do not burst.

bit 28..24: unused

must be zero

bit 23 ... 0: payload size in words

ADDRESS:

bit 31.. 0: Bus start address of the transfer.

DUMMY:

dummy words to fill the block. Only complete blocks are transferred, no short packages implemented.

Data:

contains the payload. The transferred amount of data is always a multiple of the block size - which is 8kBytes when using USB.
Unused buffer space after the payload data is filled with dummy data.

# User designs

Users who like to discard the CESYS bus adapters (FPGA IP + bus interface) and write their own logic to encode and decode the data stream must be aware that the specifications of the UDK3 transfer protocol will be modified and extended without prior notice. Some, but not all proposals to expand the protocol are:
Instead of aligning data to buffer limits, data might immediately follow the header. The header structure might change significantly when new features are added (video-stream, multi-camera support). A additional set of much smaller buffers with their own endpoints might be added to implement low-latency register access while high data-rate streaming takes place in parallel. When new versions of the UDK3 become available, user designs must be adopted to make them usable.

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# Revision history

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| v1.0 | February, 19 2014 | Initial release (mk). |
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# Table of contents