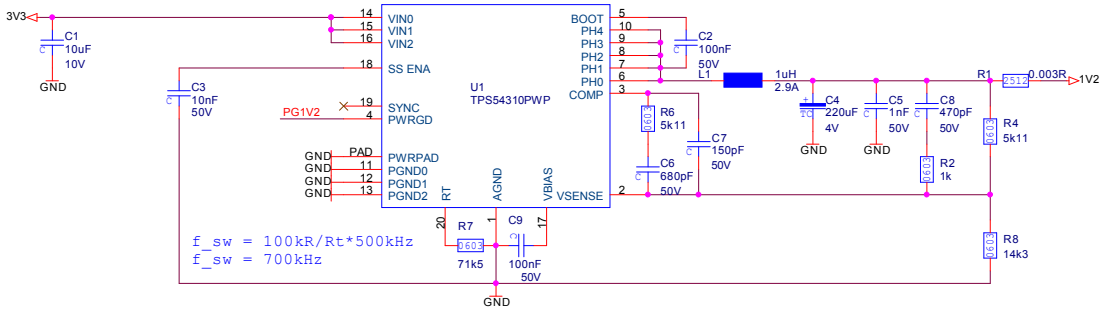
VCCINT -> VCCAUX -> VCCO

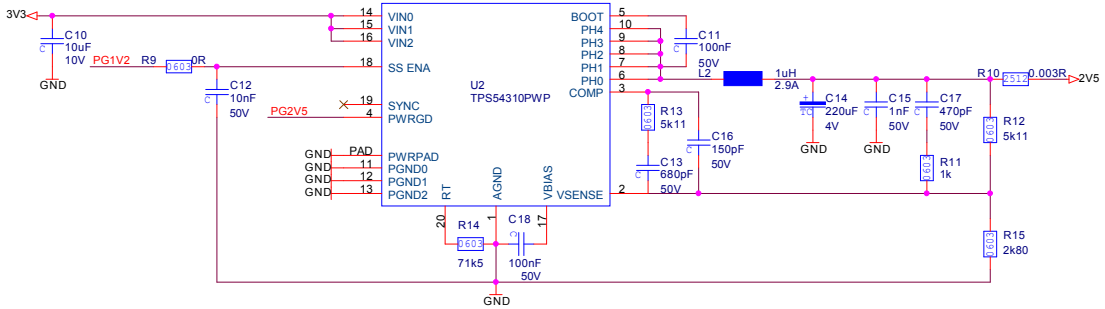
!!CAUTION!!

3V3 VCCO connected at powerup

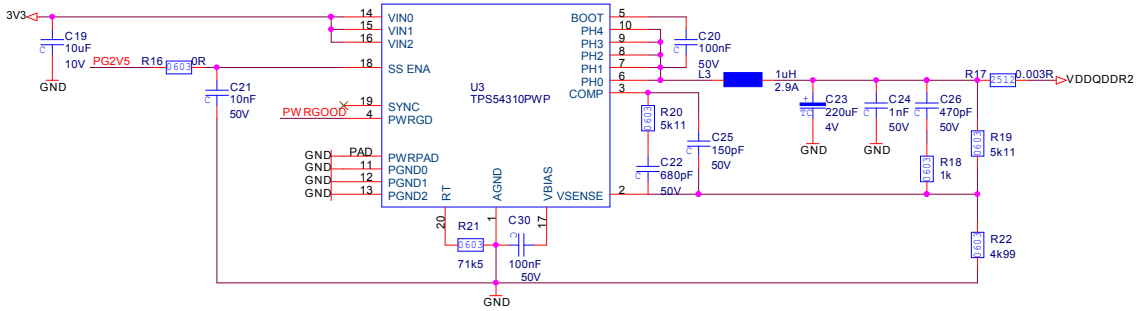
1.2VDD @ 2.9A (VCCINT)



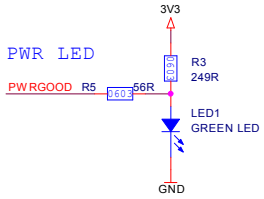
2.5VDD @ 2.9A (VCCAUX)



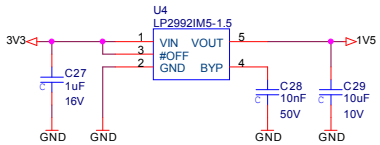
1.8VDD @ 2.9A (VCCO, VDDQ DDR2)



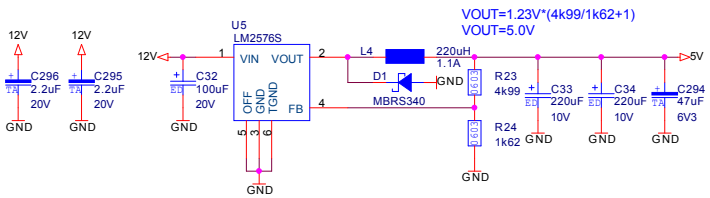
PWR LED



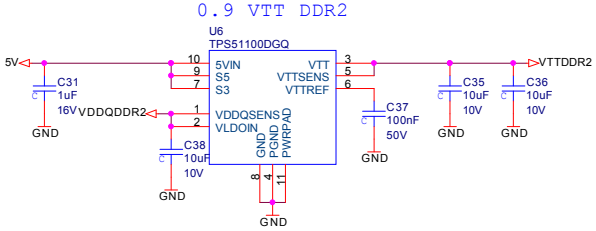
1.5VDD @ 250mA (VCORE PLX)



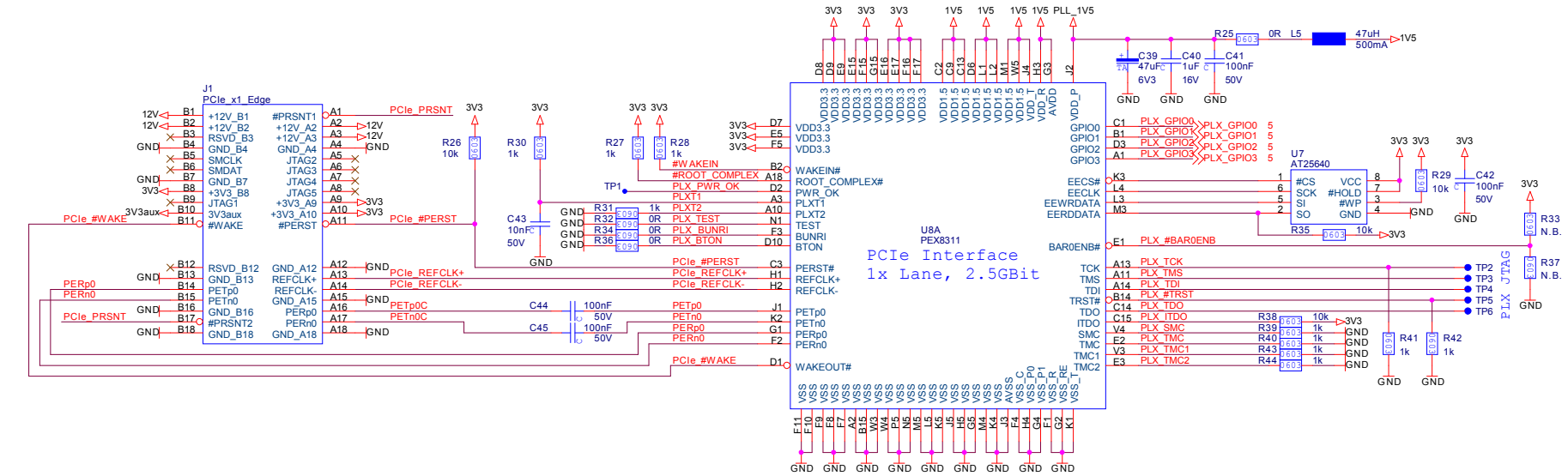
5V for PIB IF and VTTDDR2

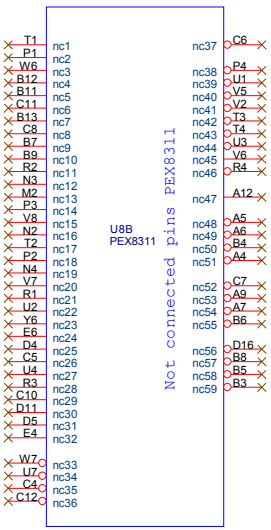


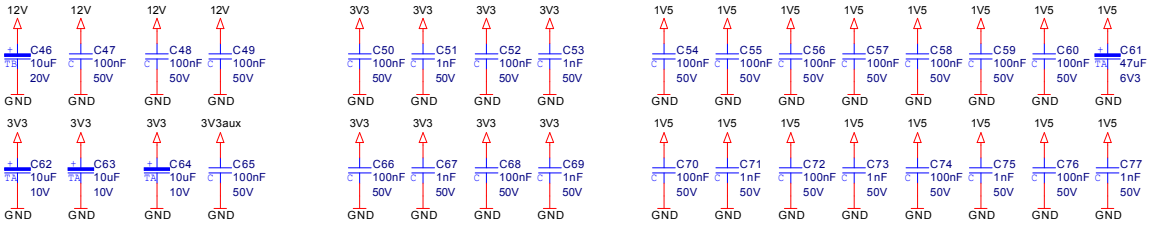
0.9 VTT DDR2



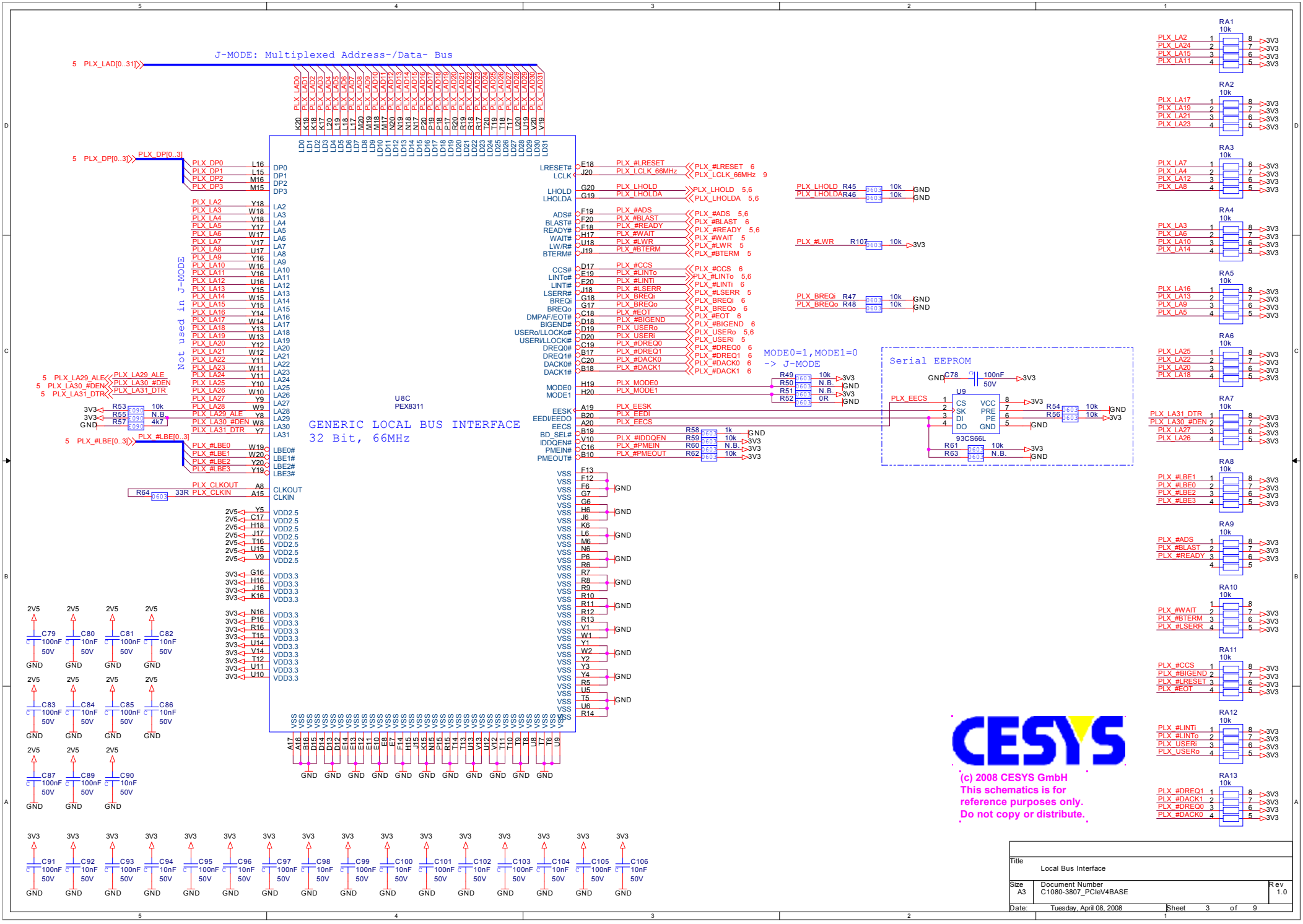
CESYS GmbH		
Title: POWER SUPPLY		
Size: A3	Document Number: C1080-3807_PCIeV4BASE	Rev: 1.0
Date: Tuesday, April 08, 2008	Sheet 1 of 9	







CESYS GmbH		
Title: PCIe Interface		
Size: A3	Document Number: C1080-3807_PCIeV4BASE	Rev: 1.0
Date: Tuesday, April 08, 2008	Sheet 2 of 9	


J-MODE: Multiplexed Address-/Data- Bus
5 PLX_LAD[0..31]
PLX_LAD0 PLX_LAD1 PLX_LAD2 PLX_LAD3 PLX_LAD4 PLX_LAD5 PLX_LAD6 PLX_LAD7 PLX_LAD8 PLX_LAD9 PLX_LAD10 PLX_LAD11 PLX_LAD12 PLX_LAD13 PLX_LAD14 PLX_LAD15 PLX_LAD16 PLX_LAD17 PLX_LAD18 PLX_LAD19 PLX_LAD20 PLX_LAD21 PLX_LAD22 PLX_LAD23 PLX_LAD24 PLX_LAD25 PLX_LAD26 PLX_LAD27 PLX_LAD28 PLX_LAD29 PLX_LAD30 PLX_LAD31
5 PLX_DP[0..3]
PLX_DP[0..3]
PLX_DP0 PLX_DP1 PLX_DP2 PLX_DP3
Not used in J-MODE
PLX_LA2 PLX_LA3 PLX_LA4 PLX_LA5 PLX_LA6 PLX_LA7 PLX_LA8 PLX_LA9 PLX_LA10 PLX_LA11 PLX_LA12 PLX_LA13 PLX_LA14 PLX_LA15 PLX_LA16 PLX_LA17 PLX_LA18 PLX_LA19 PLX_LA20 PLX_LA21 PLX_LA22 PLX_LA23 PLX_LA24 PLX_LA25 PLX_LA26 PLX_LA27 PLX_LA28 PLX_LA29_ALE PLX_LA30_#DEN PLX_LA31_DTR
5 PLX_LA29_ALE
5 PLX_LA30_#DEN
5 PLX_LA31_DTR
R53 R55 R57 10k N.B 4k7
5 PLX_#LBE[0..3]
PLX_#LBE0 PLX_#LBE1 PLX_#LBE2 PLX_#LBE3
PLX_CLKOUT
R64 33R PLX_CLKIN
U8C
PEX8311
GENERIC LOCAL BUS INTERFACE
32 Bit, 66MHz
LRESET# LCLK LHOLD LHOLDA ADS# BLAST# READY# WAIT# LW/R# BTERM# CCS# LINTo# LINTi# LSERR# BREQi BREQo DMPAF/EOT# BIGEND# USERo/LLOCKo# USERi/LLOCKi# DREQ0# DREQ1# DACK0# DACK1# MODE0 MODE1 EESK EEDI/EEDO EECS BD_SEL# IDDQEN# PMEIN# PMEOUT#
PLX_#LRESET PLX_LCLK_66MHz PLX_LHOLD PLX_LHOLDA PLX_#ADS PLX_#BLAST PLX_#READY PLX_#WAIT PLX_#LWR PLX_#BTERM PLX_#CCS PLX_#LINTo PLX_#LINTi PLX_#LSERR PLX_BREQi PLX_BREQo PLX_#EOT PLX_#BIGEND PLX_USERo PLX_USERi PLX_#DREQ0 PLX_#DREQ1 PLX_#DACK0 PLX_#DACK1 PLX_MODE0 PLX_MODE1 PLX_EESK PLX_EEDI PLX_EECS PLX_#IDDQEN PLX_#PMEIN PLX_#PMEOUT
PLX_#LRESET 6
PLX_LCLK_66MHz 9
PLX_LHOLD 5,6
PLX_LHOLDA 5,6
PLX_#ADS 5,6
PLX_#BLAST 6
PLX_#READY 5,6
PLX_#WAIT 5
PLX_#LWR 5
PLX_#BTERM 5
PLX_#CCS 6
PLX_#LINTo 5,6
PLX_#LINTi 6
PLX_#LSERR 5
PLX_BREQi 6
PLX_BREQo 6
PLX_#EOT 6
PLX_#BIGEND 6
PLX_USERo 5,6
PLX_USERi 5
PLX_#DREQ0 6
PLX_#DREQ1 6
PLX_#DACK0 6
PLX_#DACK1 6
MODE0=1,MODE1=0
-> J-MODE
R49 R50 R51 R52 10k N.B. N.B. 0R
R58 R59 R60 R62 1k 10k N.B. 10k
R45 R46 R107 R47 R48 10k
Serial EEPROM
U9
93CS66L
CS SK DI DO VCC PRE PE GND
C78 100nF 50V
R54 R56 R61 R63 10k
RA1 RA2 RA3 RA4 RA5 RA6 RA7 RA8 RA9 RA10 RA11 RA12 RA13 10k
PLX_LA2 PLX_LA24 PLX_LA15 PLX_LA11
PLX_LA17 PLX_LA19 PLX_LA21 PLX_LA23
PLX_LA7 PLX_LA4 PLX_LA12 PLX_LA8
PLX_LA3 PLX_LA6 PLX_LA10 PLX_LA14
PLX_LA16 PLX_LA13 PLX_LA9 PLX_LA5
PLX_LA25 PLX_LA22 PLX_LA20 PLX_LA18
PLX_LA31_DTR PLX_LA30_#DEN PLX_LA27 PLX_LA26
PLX_#LBE1 PLX_#LBE0 PLX_#LBE2 PLX_#LBE3
PLX_#ADS PLX_#BLAST PLX_#READY
PLX_#WAIT PLX_#BTERM PLX_#LSERR
PLX_#CCS PLX_#BIGEND PLX_#LRESET PLX_#EOT
PLX_#LINTi PLX_#LINTo PLX_USERi PLX_USERo
PLX_#DREQ1 PLX_#DACK1 PLX_#DREQ0 PLX_#DACK0
3V3 GND 2V5
C79 C80 C81 C82 C83 C84 C85 C86 C87 C89 C90 C91 C92 C93 C94 C95 C96 C97 C98 C99 C100 C101 C102 C103 C104 C105 C106
100nF 10nF 50V
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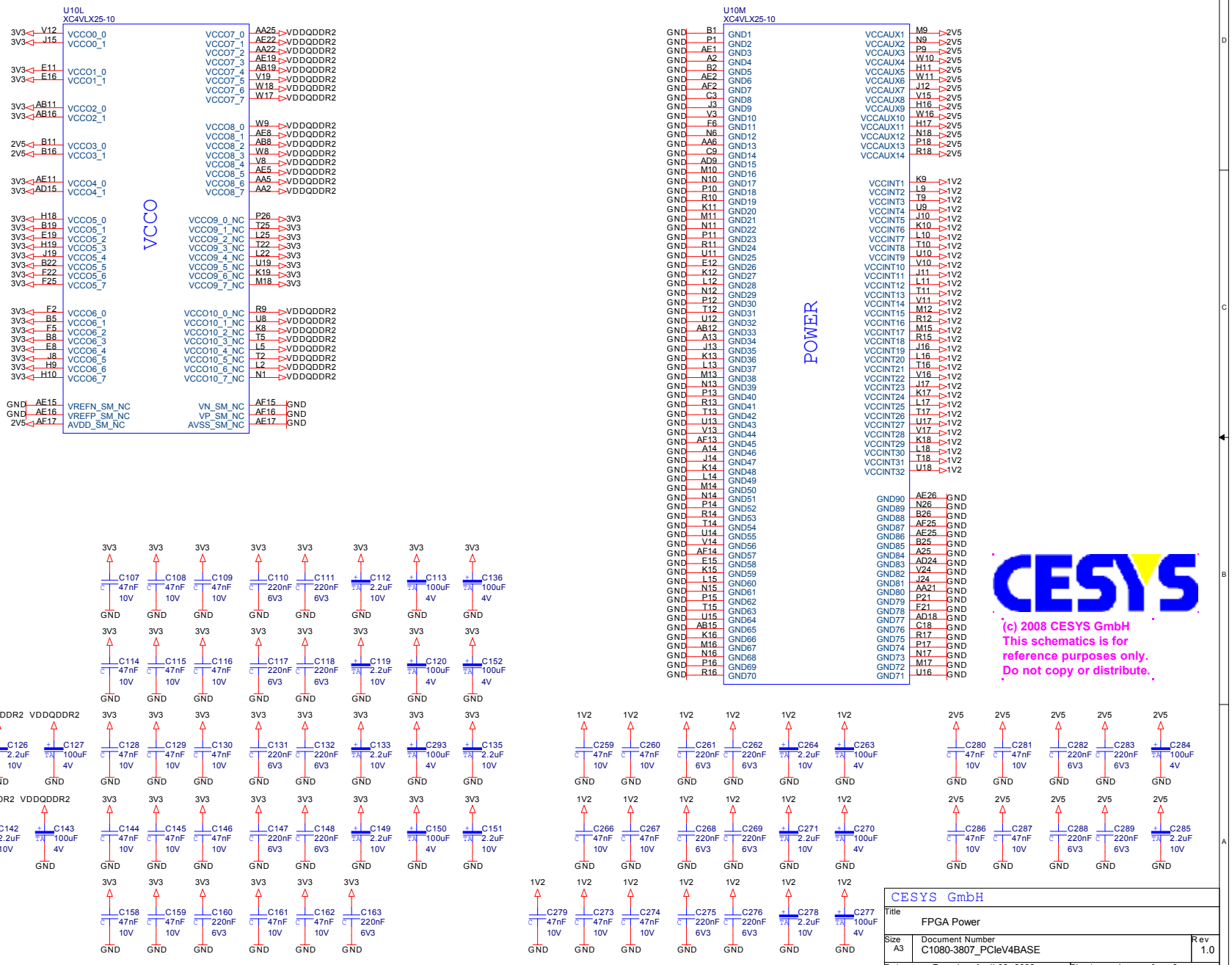
Title
Local Bus Interface
Size A3
Document Number C1080-3807_PCIeV4BASE
Rev 1.0
Date: Tuesday, April 08, 2008
Sheet 3 of 9


U10L
XC4VLX25-10
VCCO
VCCO0_0
VCCO0_1
VCCO1_0
VCCO1_1
VCCO2_0
VCCO2_1
VCCO3_0
VCCO3_1
VCCO4_0
VCCO4_1
VCCO5_0
VCCO5_1
VCCO5_2
VCCO5_3
VCCO5_4
VCCO5_5
VCCO5_6
VCCO5_7
VCCO6_0
VCCO6_1
VCCO6_2
VCCO6_3
VCCO6_4
VCCO6_5
VCCO6_6
VCCO6_7
VREFN_SM_NC
VREFP_SM_NC
AVDD_SM_NC
VCCO7_0
VCCO7_1
VCCO7_2
VCCO7_3
VCCO7_4
VCCO7_5
VCCO7_6
VCCO7_7
VCCO8_0
VCCO8_1
VCCO8_2
VCCO8_3
VCCO8_4
VCCO8_5
VCCO8_6
VCCO8_7
VCCO9_0_NC
VCCO9_1_NC
VCCO9_2_NC
VCCO9_3_NC
VCCO9_4_NC
VCCO9_5_NC
VCCO9_6_NC
VCCO9_7_NC
VCCO10_0_NC
VCCO10_1_NC
VCCO10_2_NC
VCCO10_3_NC
VCCO10_4_NC
VCCO10_5_NC
VCCO10_6_NC
VCCO10_7_NC
VN_SM_NC
VP_SM_NC
AVSS_SM_NC
VDDQDDR2
3V3
GND
U10M
XC4VLX25-10
POWER
GND1
GND2
GND3
GND4
GND5
GND6
GND7
GND8
GND9
GND10
GND11
GND12
GND13
GND14
GND15
GND16
GND17
GND18
GND19
GND20
GND21
GND22
GND23
GND24
GND25
GND26
GND27
GND28
GND29
GND30
GND31
GND32
GND33
GND34
GND35
GND36
GND37
GND38
GND39
GND40
GND41
GND42
GND43
GND44
GND45
GND46
GND47
GND48
GND49
GND50
GND51
GND52
GND53
GND54
GND55
GND56
GND57
GND58
GND59
GND60
GND61
GND62
GND63
GND64
GND65
GND66
GND67
GND68
GND69
GND70
VCCAUX1
VCCAUX2
VCCAUX3
VCCAUX4
VCCAUX5
VCCAUX6
VCCAUX7
VCCAUX8
VCCAUX9
VCCAUX10
VCCAUX11
VCCAUX12
VCCAUX13
VCCAUX14
VCCINT1
VCCINT2
VCCINT3
VCCINT4
VCCINT5
VCCINT6
VCCINT7
VCCINT8
VCCINT9
VCCINT10
VCCINT11
VCCINT12
VCCINT13
VCCINT14
VCCINT15
VCCINT16
VCCINT17
VCCINT18
VCCINT19
VCCINT20
VCCINT21
VCCINT22
VCCINT23
VCCINT24
VCCINT25
VCCINT26
VCCINT27
VCCINT28
VCCINT29
VCCINT30
VCCINT31
VCCINT32
GND90
GND89
GND88
GND87
GND86
GND85
GND84
GND83
GND82
GND81
GND80
GND79
GND78
GND77
GND76
GND75
GND74
GND73
GND72
GND71
2V5
1V2
C107 47nF 10V
C108 47nF 10V
C109 47nF 10V
C110 220nF 6V3
C111 220nF 6V3
C112 2.2uF 10V
C113 100uF 4V
C136 100uF 4V
C114 47nF 10V
C115 47nF 10V
C116 47nF 10V
C117 220nF 6V3
C118 220nF 6V3
C119 2.2uF 10V
C120 100uF 4V
C152 100uF 4V
C121 47nF 10V
C122 47nF 10V
C123 47nF 10V
C124 220nF 6V3
C125 220nF 6V3
C126 2.2uF 10V
C127 100uF 4V
C128 47nF 10V
C129 47nF 10V
C130 47nF 10V
C131 220nF 6V3
C132 220nF 6V3
C133 2.2uF 10V
C293 100uF 4V
C135 2.2uF 10V
C137 47nF 10V
C138 47nF 10V
C139 47nF 10V
C140 220nF 6V3
C141 220nF 6V3
C142 2.2uF 10V
C143 100uF 4V
C144 47nF 10V
C145 47nF 10V
C146 47nF 10V
C147 220nF 6V3
C148 220nF 6V3
C149 2.2uF 10V
C150 100uF 4V
C151 2.2uF 10V
C153 47nF 10V
C154 47nF 10V
C155 220nF 6V3
C156 2.2uF 10V
C157 100uF 4V
C158 47nF 10V
C159 47nF 10V
C160 220nF 6V3
C161 47nF 10V
C162 47nF 10V
C163 220nF 6V3
C259 47nF 10V
C260 47nF 10V
C261 220nF 6V3
C262 220nF 6V3
C264 2.2uF 10V
C263 100uF 4V
C266 47nF 10V
C267 47nF 10V
C268 220nF 6V3
C269 220nF 6V3
C271 2.2uF 10V
C270 100uF 4V
C279 47nF 10V
C273 47nF 10V
C274 47nF 10V
C275 220nF 6V3
C276 220nF 6V3
C278 2.2uF 10V
C277 100uF 4V
C280 47nF 10V
C281 47nF 10V
C282 220nF 6V3
C283 220nF 6V3
C284 100uF 4V
C286 47nF 10V
C287 47nF 10V
C288 220nF 6V3
C289 220nF 6V3
C285 2.2uF 10V
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CESYS GmbH
Title
FPGA Power
Size
A3
Document Number
C1080-3807_PCIeV4BASE
Rev
1.0
Date:
Tuesday, April 08, 2008
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of
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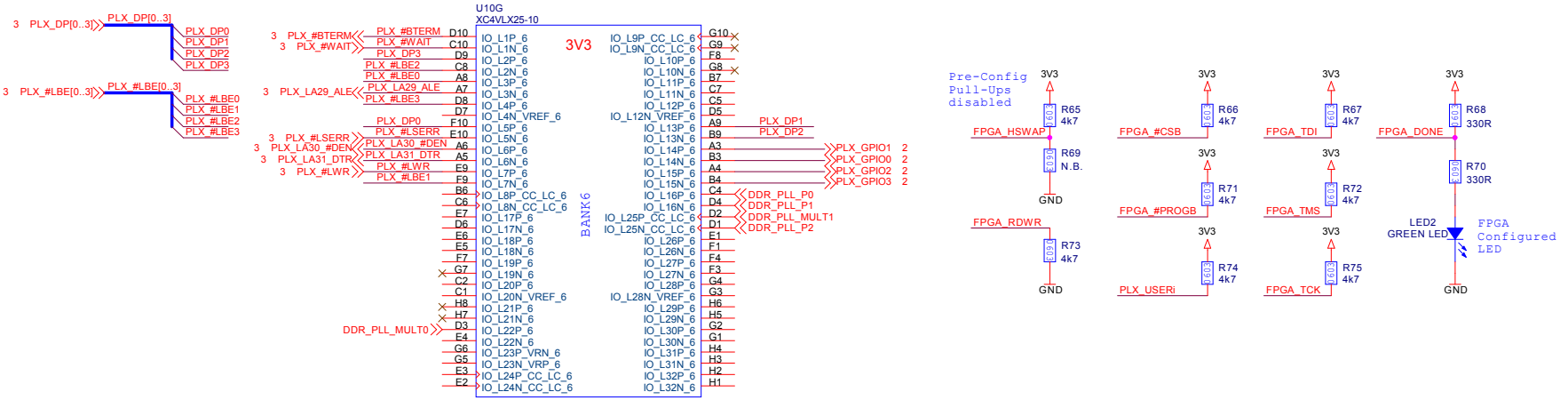
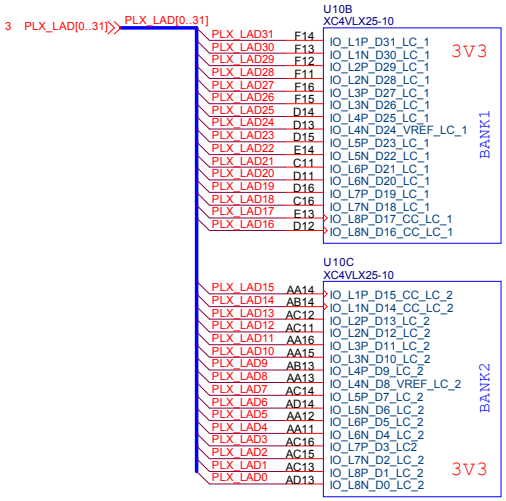
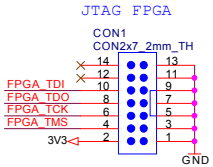
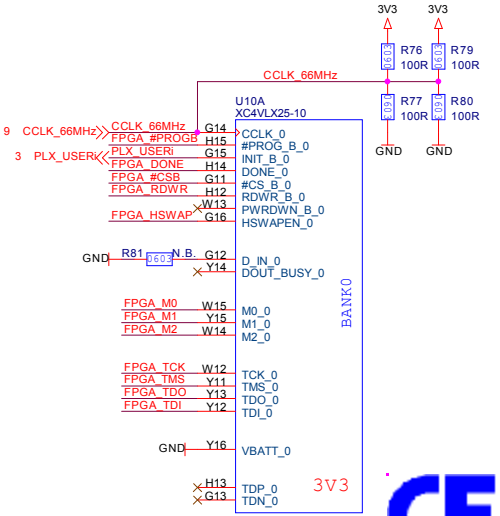


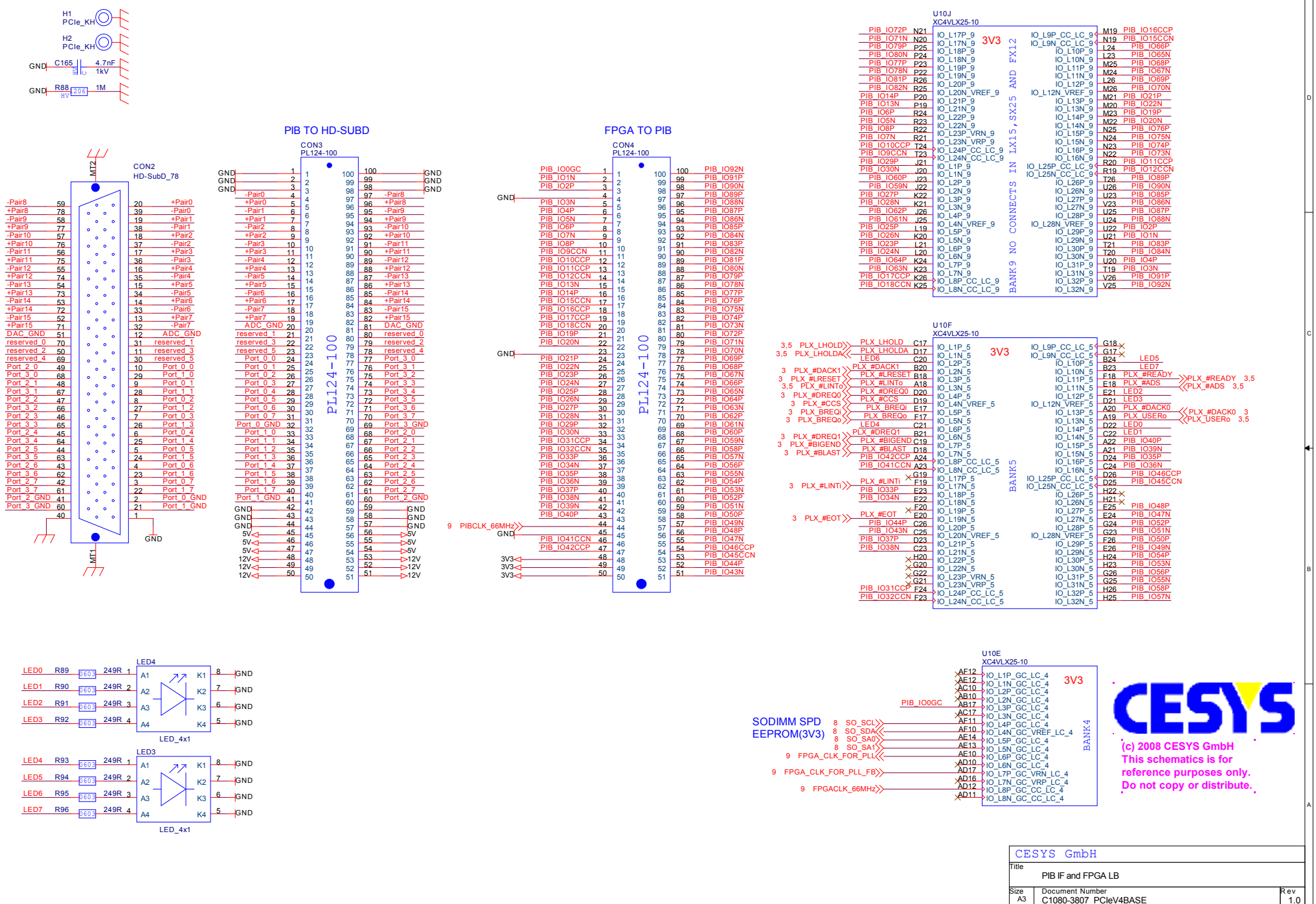


Some confidential information removed here ...





CESYS GmbH		
Title: FPGA Config and LB		
Size: A3	Document Number: C1080-3807_PCIeV4BASE	Rev: 1.0
Date: Tuesday, April 08, 2008	Sheet 5 of 9	


H1
PCIe_KH
H2
PCIe_KH
GND
C165
4.7nF
1kV
GND
R88
206
1M
CON2
HD-SubD_78
MT2
MT1
GND
PIB TO HD-SUBD
CON3
PCB124-100
FPGA TO PIB
CON4
PCB124-100
U10J
XC4VLX25-10
3V3
BANK9 NO CONNECTS IN LX15, SX25 AND FX12
U10F
XC4VLX25-10
3V3
BANK5
U10E
XC4VLX25-10
3V3
BANK4
LED4
LED_4x1
LED3
LED_4x1
SODIMM SPD
EEPROM(3V3)
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Title
PIB IF and FPGA LB
Size
A3
Document Number
C1080-3807_PCIeV4BASE
Rev
1.0
Date:
Tuesday, April 08, 2008
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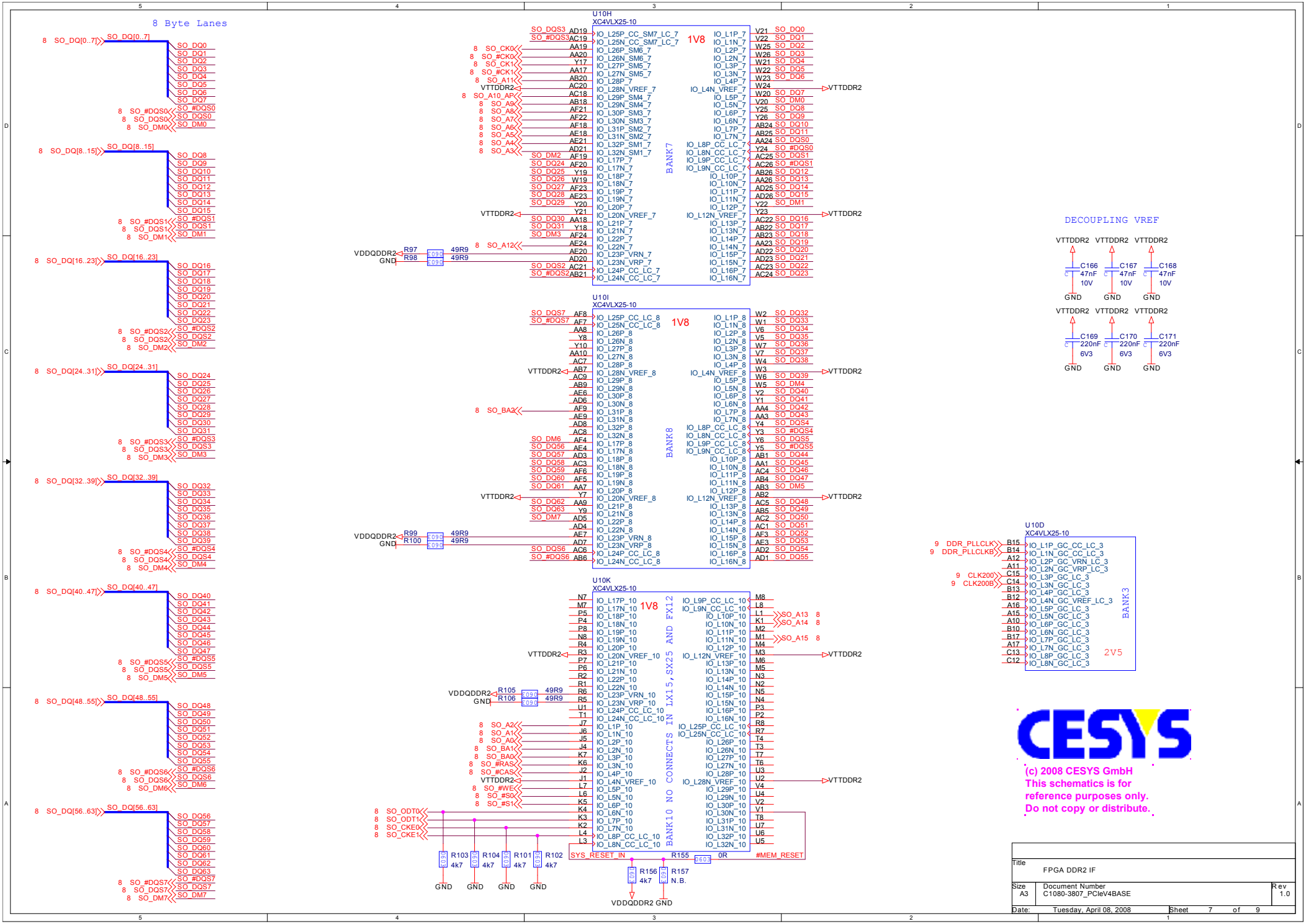
8 Byte Lanes
U10H
XC4VLX25-10
U10I
XC4VLX25-10
U10K
XC4VLX25-10
U10D
XC4VLX25-10
1V8
2V5
BANK7
BANK8
BANK10
BANK3
NO CONNECTS IN LX15, SX25 AND FX12
DECOUPLING VREF
VTTDDR2
VDDQDDR2
GND
SYS_RESET_IN
#MEM_RESET
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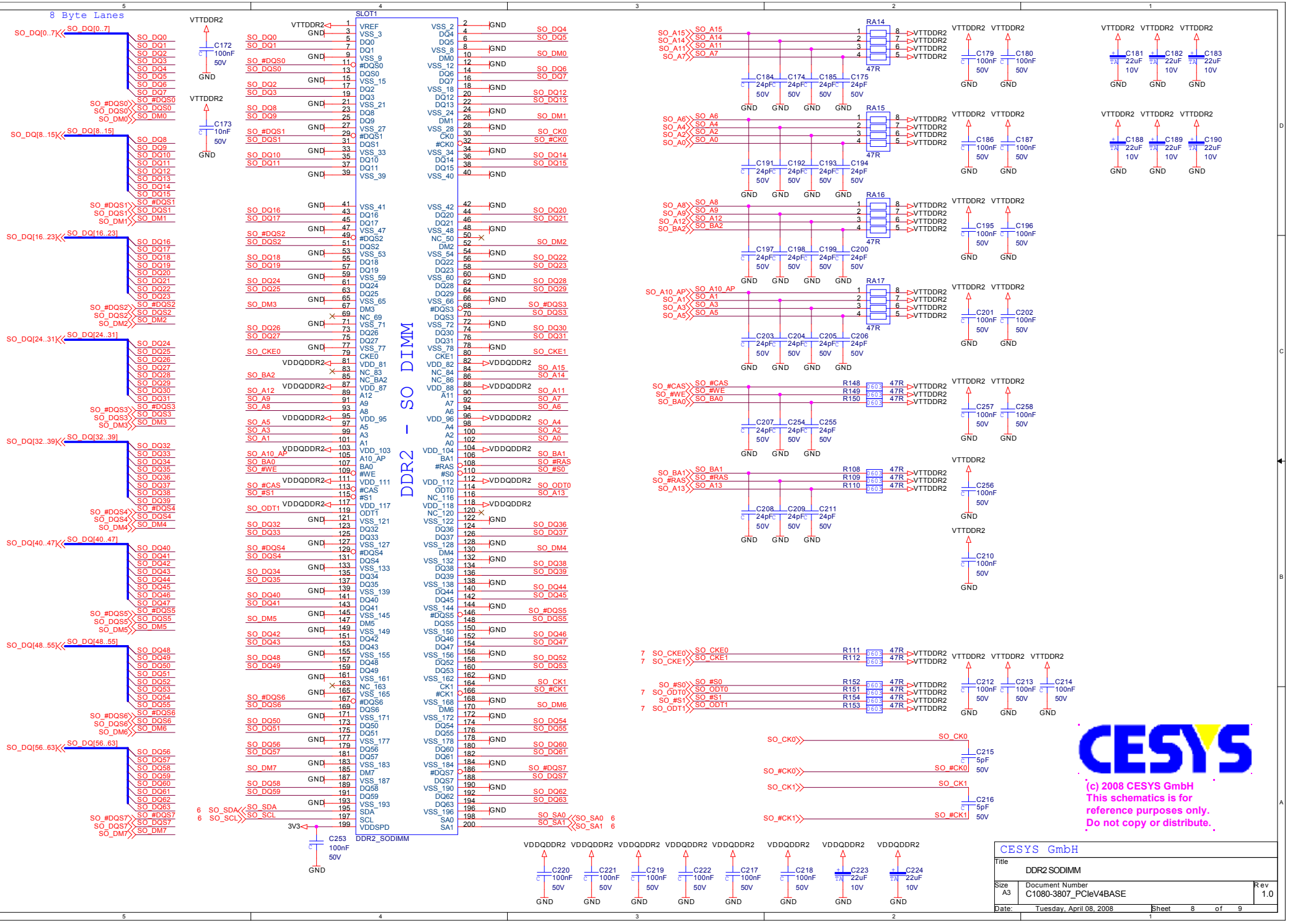
Title
FPGA DDR2 IF
Size A3
Document Number C1080-3807_PCIeV4BASE
Rev 1.0
Date: Tuesday, April 08, 2008
Sheet 7 of 9


8 Byte Lanes
SLOT1
DDR2 - SO DIMM
DDR2_SODIMM
VTTDDR2
VDDQDDR2
GND
3V3
47R
RA14
RA15
RA16
RA17
R148
R149
R150
R108
R109
R110
R111
R112
R152
R151
R154
R153
C253 100nF 50V
C172 100nF 50V
C173 10nF 50V
C179 100nF 50V
C180 100nF 50V
C181 22uF 10V
C182 22uF 10V
C183 22uF 10V
C184 24pF 50V
C174 24pF 50V
C185 24pF 50V
C175 24pF 50V
C186 100nF 50V
C187 100nF 50V
C188 22uF 10V
C189 22uF 10V
C190 22uF 10V
C191 24pF 50V
C192 24pF 50V
C193 24pF 50V
C194 24pF 50V
C195 100nF 50V
C196 100nF 50V
C197 24pF 50V
C198 24pF 50V
C199 24pF 50V
C200 24pF 50V
C201 100nF 50V
C202 100nF 50V
C203 24pF 50V
C204 24pF 50V
C205 24pF 50V
C206 24pF 50V
C257 100nF 50V
C258 100nF 50V
C207 24pF 50V
C254 24pF 50V
C255 24pF
C256 100nF 50V
C208 24pF 50V
C209 24pF 50V
C211 24pF
C210 100nF 50V
C212 100nF 50V
C213 100nF 50V
C214 100nF 50V
C215 5pF 50V
C216 5pF 50V
C220 100nF 50V
C221 100nF 50V
C219 100nF 50V
C222 100nF 50V
C217 100nF 50V
C218 100nF 50V
C223 22uF 10V
C224 22uF 10V
SO_DQ[0..7]
SO_DQ[8..15]
SO_DQ[16..23]
SO_DQ[24..31]
SO_DQ[32..39]
SO_DQ[40..47]
SO_DQ[48..55]
SO_DQ[56..63]
SO_#DQS0
SO_DQS0
SO_DM0
SO_#DQS1
SO_DQS1
SO_DM1
SO_#DQS2
SO_DQS2
SO_DM2
SO_#DQS3
SO_DQS3
SO_DM3
SO_#DQS4
SO_DQS4
SO_DM4
SO_#DQS5
SO_DQS5
SO_DM5
SO_#DQS6
SO_DQS6
SO_DM6
SO_#DQS7
SO_DQS7
SO_DM7
SO_SDA
SO_SCL
SO_A15
SO_A14
SO_A11
SO_A7
SO_A6
SO_A4
SO_A2
SO_A0
SO_A8
SO_A9
SO_A12
SO_BA2
SO_A10_AP
SO_A1
SO_A3
SO_A5
SO_#CAS
SO_#WE
SO_BA0
SO_BA1
SO_#RAS
SO_A13
SO_CKE0
SO_CKE1
SO_#S0
SO_ODT0
SO_#S1
SO_ODT1
SO_CK0
SO_#CK0
SO_CK1
SO_#CK1
SO_SA0
SO_SA1
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Title
DDR2 SODIMM
Size A3
Document Number C1080-3807_PCIeV4BASE
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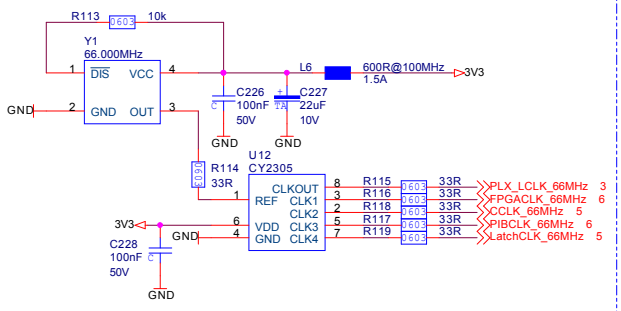
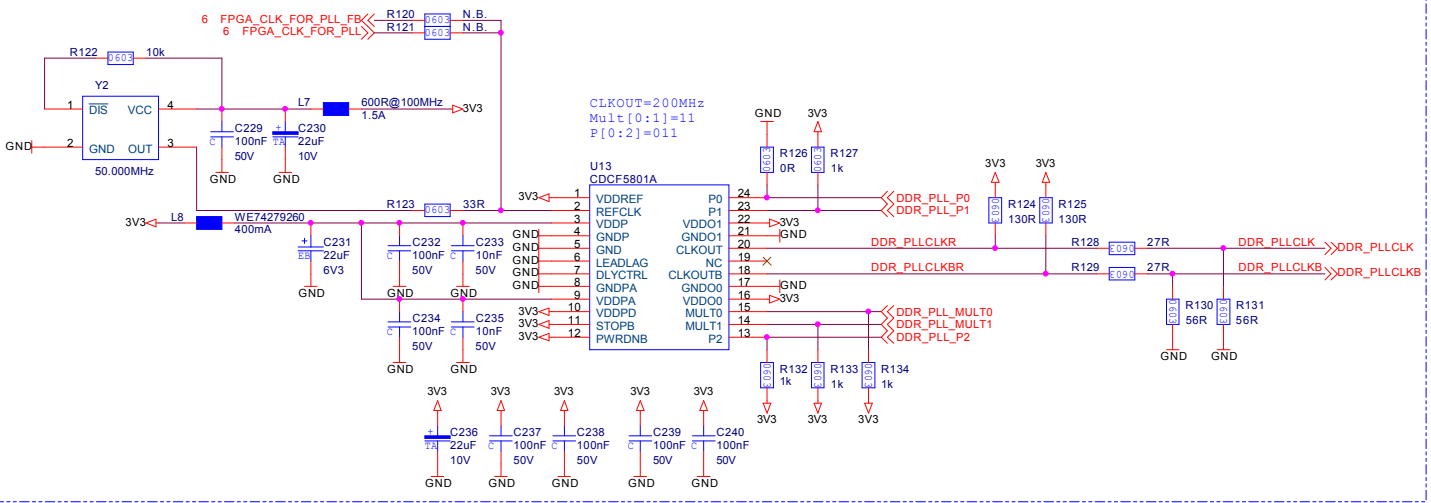
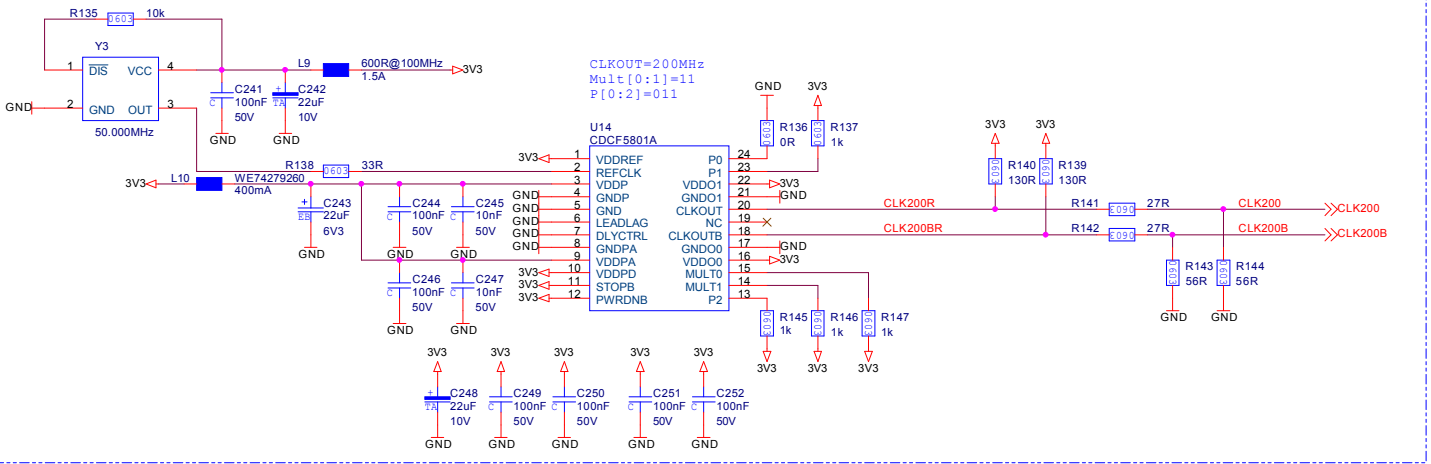
Clock Distribution 66MHz



DDR2 clock (LVPECL25 compatible) via PLL with external reference clock.
Optional an FPGA clock can be used as reference clock.



200MHz clock for idelay (LVPECL25 compatible)



Title	CLOCK	
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