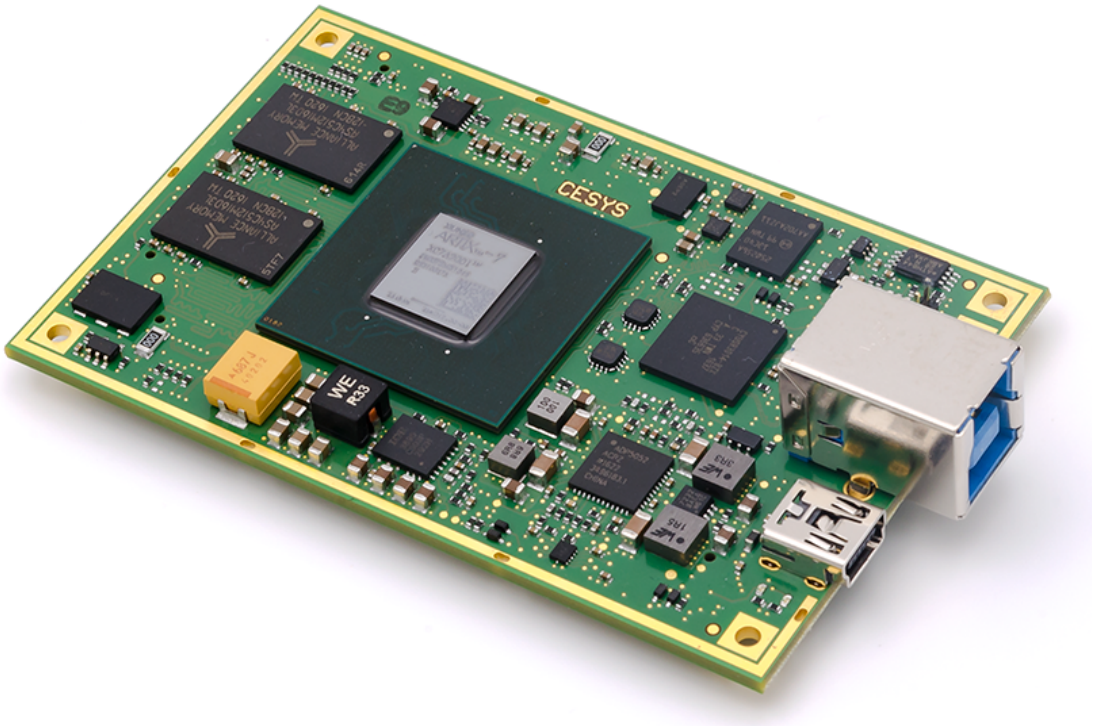
White Paper: EFM-03 Beastboard

Bit Error Rate Test for EFM-03 GTP Columns



Overview

The EFM-03 Beastboard is equipped with a Xilinx Artix-7 XC7A200T-2FBG676I FPGA. This device consists of eight Gigabit Transceiver Ports (GTP), classified into 2 modules, each containing 4 GTP channels and 2 Common modules collectively reffered to as GTP Quads. Each Quad consists of 4 serial transceivers (GTP Channels) and 2 dedicated clock pins (GTP Commons) that are internally hardwired to 2 PLLs. It is not mandatory to use both the clock paths. A single reference clock can be shared across the 4 chanels present in that particular Quad. These ports are high-speed differential serial interfaces designed with specific hardware at chip level and are routed to FPGA balls over dedicated paths. They are capable of a line rate of upto 6.6 Gigabits per second (Gbps). While this powerful device can deliver data transfers at such high speeds, setting up a design which instantiates the respective primitives and testing them for proper functionality in real hardware is a challenging task.

This Whitepaper presents a standard method to verify the functionality of the GTP modules and also to verify the Physical Medium for an error-free data transfer. The method used to accomplish this is the Bit Error Rate Test (BERT) approach. A functional verification process of the GTP and the physical medium is described in this paper. The GTP quads in EFM-03 Beastboard, ultimately on the Artix-7 FPGA, are tested with the “IBERT 7-Series GTP” IP Core from Xilinx with different line using HDMI cable as the physical medium. The paper presents the hardware requirements, test setup, test process, test results and a brief analysis of the results.

System Requirements

- EFM-03 Beastboard, CESYS, EFM03-200T-2I
- EFM-03 Breakout Board revision A.1
- 1x Texas Instruments LMK61PDEVM clock oscillator Evaluation module[1]
- 2x SMA male-to-male cable
- 1x HDMI male-to-male cable
- Windows-PC running 64-bit Windows OS
- Vivado Design Suite (2017.2.1 onwards)
- Xilinx Platform Cable USB-II

IMPORTANT NOTE: Xilinx recommends the usage of reference clocks whose Phase-Noise ratio masks for QPLL and CPLL fall in the range as specified below. If these recommendations are not followed, The GTP's internal clocks will not be locked and consequentially, the GTPs will fail to initialize rendering the channels unusable.

QPLL:

Reference Clock (MHz)	Phase-Noise Ratio at Offset Frequency (dBc/Hz)		
	10 kHz	100 kHz	1 MHz
100	-126	-130	-134
125	-123	-129	-133
156.25	-122	-127	-132
250	-119	-126	-131
312.5	-115	-124	-130
625	-110	-116	-120

CPLL:

Reference Clock (MHz)	Phase-Noise Ratio at Offset Frequency (dBc/Hz)		
	10 kHz	100 kHz	1 MHz
100	-126	-132	-136
125	-123	-131	-135
156.25	-122	-129	-133
250	-119	-126	-132
312.5	-116	-124	-131
625	-110	-119	-127

1 LMK61PDEVM or any other clock oscillator module capable of providing a low phase jitter in accordance with the values in tables above can be used.

Test Setup

Due to availability of only one external clock oscillator module, two tests are conducted one after the other in order to test both the GTP Quads for proper functionality. The below figure shows the test setup that was used for testing GTP Quad 216 to verify its functionality and consequentially the physical medium. Please make sure all the connections are made as shown in the Figure 1 before powering-up the EFM-03 module.

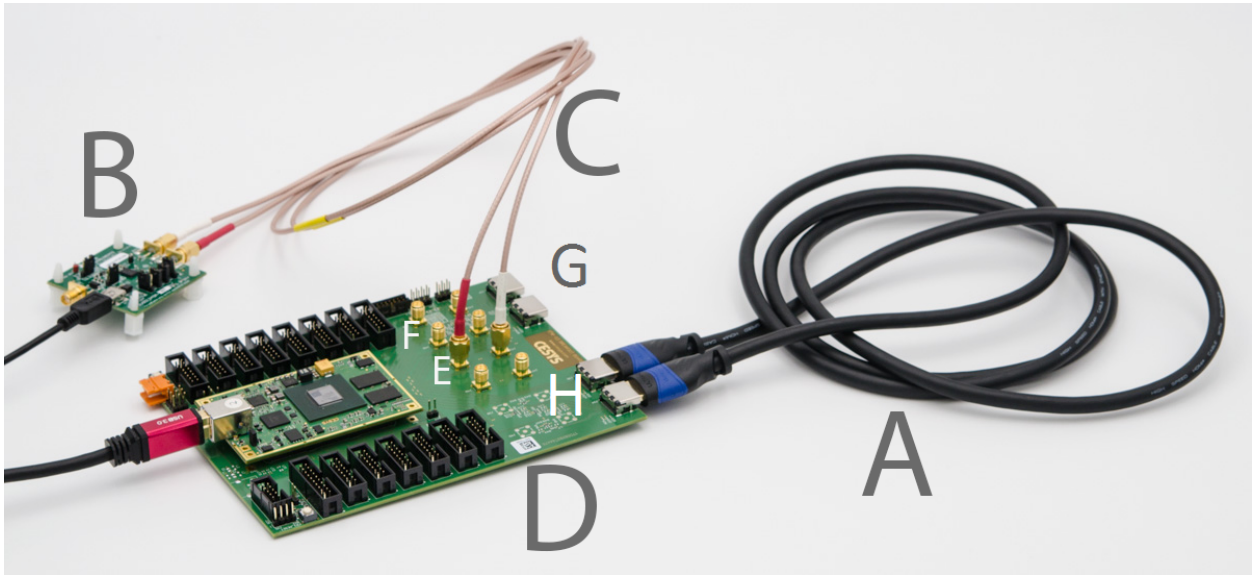


Figure 1: Test Setup for verifying GTP Quad 216

A) The physical loopback using the HDMI cable

B) LMK61PDEVM clock oscillator evaluation module

C) SMA Cables providing the 125MHz Differential Reference Clock

D) EFM-03 Breakout Board with the EFM-03 Beastboard installed on it

E) Differential clock inputs J42 (refclk_p) and J43 (refclk_n) for MGTREFCLK0 216

F) Differential clock inputs J44 (refclk_p) and J45 (refclk_n) for MGTREFCLK0 213

G) Ports for GTP 216 serial transceivers

H) Ports for GTP 213 serial transceivers

The EFM-03 module is plugged onto the EFM-03 Breakout board by means of the high-speed Samtec connectors. The Breakout board routes the highspeed serial transceivers to 4 HDMI female connectors. The reference clocks pins are routed to the female SMA connectors on the Breakout board. The below table shows how the GTP ports are connected.

Quad	GTP Channel	TX		RX	
		TX_P	TX_N	RX_P	RX_N
MGT_213	X0Y0	J36 - 1	J36 - 3	J37 - 4	J37 - 6
	X0Y1	J36 - 4	J36 - 6	J37 - 7	J37 - 9
	X0Y2	J36 - 10	J36 - 12	J37 - 1	J37 - 3
	X0Y3	J36 - 7	J36 - 9	J37 – 10	J37 - 12
MGT_216	X0Y4	J35 - 4	J35 - 6	J34 - 4	J34 - 6
	X0Y5	J35 - 1	J35 - 3	J34 – 10	J34 - 12
	X0Y6	J35 – 10	J35 - 12	J34 – 7	J34 - 9
	X0Y7	J35 – 7	J35 - 9	J34 – 1	J34 - 3

Please refer to *ug-120-EFM-03-hardware-reference.pdf* at the below link for further details:

https://www.cesys.com/en/service-support/download-center/fpga.html

Once the test for Quad 216 is completed, please connect the clock source to the SMA connectors denoted in the figure under **F** (J44 and J45) in the image. Also, please connect the HDMI cable between the remaining two GTP ports denoted in the figure under **G**.

Generating the IBERT IP Core

The test uses the “IBERT 7-Series GTP” IP core to functionally verify the GTP modules. To generate the FPGA design for this test, please follow the below steps:

- Open Vivado Design Suite (2017.2.1 onwards)
- Create a new project by clicking **Create Project** under **Quick Start** tab with xc7a200tfbg676-2 as the part.
- Open the **IP Catalog** under **PROJECT MANAGER** tab
- Select **IBERT 7 Series GTP** IP Core under “Debug & Verification → Debug”
- Double-click on the IP core and customize with below parameters
  - Protocol Definition tab
    - Select General ES/Production
    - Number of Protocols : 1 (See **NOTE** below)
    - Protocol - Custom 1
      - LineRate(Gbps) : 6.25
      - Data Width : 16
      - RefClk(MHz) : 125.000
      - Quad Count : 1
      - PLL Used : PLL0
  - Protocol Selection tab
    - QUAD_213 / QUAD_216
      - Protocol Selected : Custom 1/ 6.25 Gbps
      - RefClk Selection : MGTREFCLK0 213 / MGTREFCLK0 216
      - TXUSRCLK Source : Channel 0

    Only one of the 2 quads can be configured at a time. Please select the appropriate MGTREFCLK0 for RefClk selection. See **NOTE** below.
  - Clock Settings tab
      - Clock Type : System Clock
      - Source : External

- I/O Standard : DIFF_SSTL_15
- P Package Pin : R3
- N Package Pin : P3
- Frequency(MHz) : 200

- Click **OK** and in the Generate Output Products pop-up, click **Generate**

IMPORTANT NOTE : At the time of writing this paper, only one Clock Oscillator Module was available and therefore only one of the two GTP Quads could be tested at a time. If users have more than one external clock modules capable of providing a differential clock complying with the Phase-Noise masks described earlier (System Requirements), both Quads can be tested simultaneously. Instead of selecting Number of Protocols as '1', users can select '2'. Also, please make sure to change the settings on the **Protocol Selection** tab.

Generating the IP example design

- Right-click on the above generated IP (.XCI) file in **Sources** window and select **Open IP Example Design…**
- Check the project path and press **OK**
- A **new Vivado project will be opened automatically** with an example design for the IBERT 7 Series IP core.
- Click **Generate Bitstream** under **PROGRAM AND DEBUG** tab
- Once the Bitstream is generated, click on **Open Hardware Manager** which will open the Vivado hardware manager.
- Click on **Open Target → Auto Connect**
- Right-click on xc7a200t_0 (the device) and select **Program Device…**
- Select the bitstream you generated and click **Program**

IMPORTANT NOTE : After completely testing one of the GTP Quads, please regenarate the IP Core described under "Generating the IBERT IP Core" with settings for the other GTP Quad.

Test Results

Checking the data transfer

After programming the FPGA, on the top left corner of the Hardware Manager, select Auto-Detect Links as shown in Figure 2.

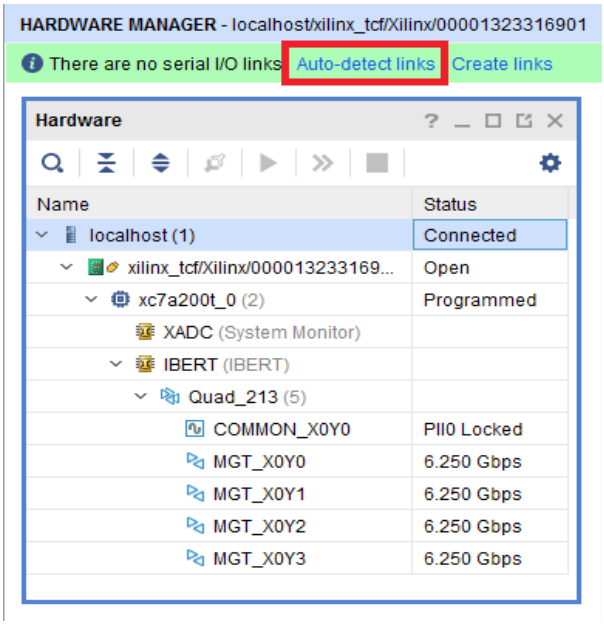


Figure 2 : Auto-detect links illustration

The IBERT Core automatically sets up the links between the 4 GTP channels and generates a Slow-clock data pattern (10xClock => 11111111110000000000) and transmits it through the TX Channels. It receives the Slow-clock pattern on the RX Channels and checks the received bits for errors. Navigate to Serial I/O Links tab. Four Links should be found and the window looks similar to the illustration shown in Figure 3. Figure 4 shows the Serial I/O Links tab for the tests with GTP Quad 216.

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Li...															
Found Links (4)							Reset	Slow Clk	Slow Clk	Inject	Reset	Reset			None
Found 0	MGT_X0Y1/TX	MGT_X0Y0/RX	6.250 Gbps	1.184E12	0E0	8.446E-13	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 1	MGT_X0Y3/TX	MGT_X0Y1/RX	6.250 Gbps	1.184E12	0E0	8.445E-13	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 2	MGT_X0Y0/TX	MGT_X0Y2/RX	6.250 Gbps	1.184E12	0E0	8.444E-13	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 3	MGT_X0Y2/TX	MGT_X0Y3/RX	6.253 Gbps	1.184E12	0E0	8.445E-13	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None

Figure 3 : Serial I/O Links test parameters and results for GTP Quad 213

Tcl Console | Messages | Serial I/O Links | Serial I/O Scans

Name	TX	RX	Status	Bits	Errors	BER	BERT Reset	TX Pattern	RX Pattern	Inject Error	TX Reset	RX Reset	RX PLL Status	TX PLL Status	Loopback Mode
Ungrouped Li...															
Found Links (4)							Reset	Slow Clk	Slow Clk	Inject	Reset	Reset			None
Found 0	MGT_X0Y4/TX	MGT_X0Y4/RX	6.250 Gbps	2.659E11	0E0	3.761E-12	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 1	MGT_X0Y6/TX	MGT_X0Y5/RX	6.250 Gbps	2.659E11	0E0	3.76E-12	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 2	MGT_X0Y7/TX	MGT_X0Y6/RX	6.250 Gbps	2.659E11	0E0	3.761E-12	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None
Found 3	MGT_X0Y5/TX	MGT_X0Y7/RX	6.250 Gbps	2.659E11	0E0	3.761E-12	Reset	Slow Clk	Slow Clk	Inject	Reset	Reset	Locked	Locked	None

Figure 4 : Serial I/O links test parameters and results for GTP Quad 216

The **Status** tab must be green for all the links and should display the line rate that was selected during the IP Core generation process, in this case 6.25Gbps. This indicates the Link is up and running. The **Errors** tab must be 0E0. The **BER** (Bit Error Rate) tab usually contains the value:

$$Errors+1 \Big/ Bits$$

User can also inject errors manually in the system by clicking on the **Inject** button. One can reset the TX and RX FSMs by clicking on respective **BERT Reset** buttons shown in red boxes. User can also test the GTPs in 4 different loopback configurations and data patterns other than Slow-Clock pattern can also be selected in the dropdown menu. Please make sure to press **BERT Reset** or **TX Reset and RX Reset** buttons shown in red boxes if any parameters are changed. For our test purposes, the system was connected in a physical loopback configuration, no internal loobacks were selected. Please refer to "*PG168 7 Series FPGAs Transceivers Wizard v3.6"* for more details.

BERT Analysis with EyeScans

An eye diagram is a useful tool for understanding signal integrity in the physical layer of high-speed digital data systems. It can be used to verify the transmitter's output compliance and reveal the amplitude and time distortion in elements that can potentially degrade the BER in the received symbols. The 7 series FPGAs GTP transceivers' RX-EyeScan provides a mechanism to measure and visualize the receiver Eye margin after the RX equalizer stage. Additional usage modes enable several other methods to determine and diagnose the effects of equalization settings. The opening of the *Statistical Eye* denotes the integrity of the received signal. If the analysis yields a wide Eye, it means that the received signal has a high quality and low distortion. Similarly, a narrower eye denotes a highly distorted signal. A closed eye (no eye) denotes a lot of errors in the received signal and user must check the physical medium for faults. Please refer to RX Margin Analysis section in *UG482 7 Series FPGAs GTP Transceivers User Guide* for further details.

In order to generate Eye scans for the IBERT design, navigate to the **Serial I/O Scans** window in Vivado Hardware Manager and click on **Create Scans**. In the pop-up, set the different parameters and press OK. An EyeScan test will be performed on the selected loopback link. Each Quad was tested with a line rate of 6.25Gbps and the test results and Eyescan results are presented in the next section.

Test and EyeScan results with different line rates

The EyeScans were performed with Slow-clock pattern being transmitted and received over the links. The links are connected in physical loopback as shown in the table.

MGT quad 213 loopback links				MGT quad 216 loopback links			
Link Number	Line Rate (Gbps)	TX Channel	RX Channel	Link Number	Line Rate (Gbps)	TX Channel	RX Channel
0	6.25	MGT_X0Y1	MGT_X0Y0	0	6.25	MGT_X0Y4	MGT_X0Y4
1	6.25	MGT_X0Y3	MGT_X0Y1	1	6.25	MGT_X0Y6	MGT_X0Y5
2	6.25	MGT_X0Y0	MGT_X0Y2	2	6.25	MGT_X0Y7	MGT_X0Y6
3	6.25	MGT_X0Y2	MGT_X0Y3	3	6.25	MGT_X0Y5	MGT_X0Y7

The GTP Quad 213 EyeScan results for all four channels are presented below.

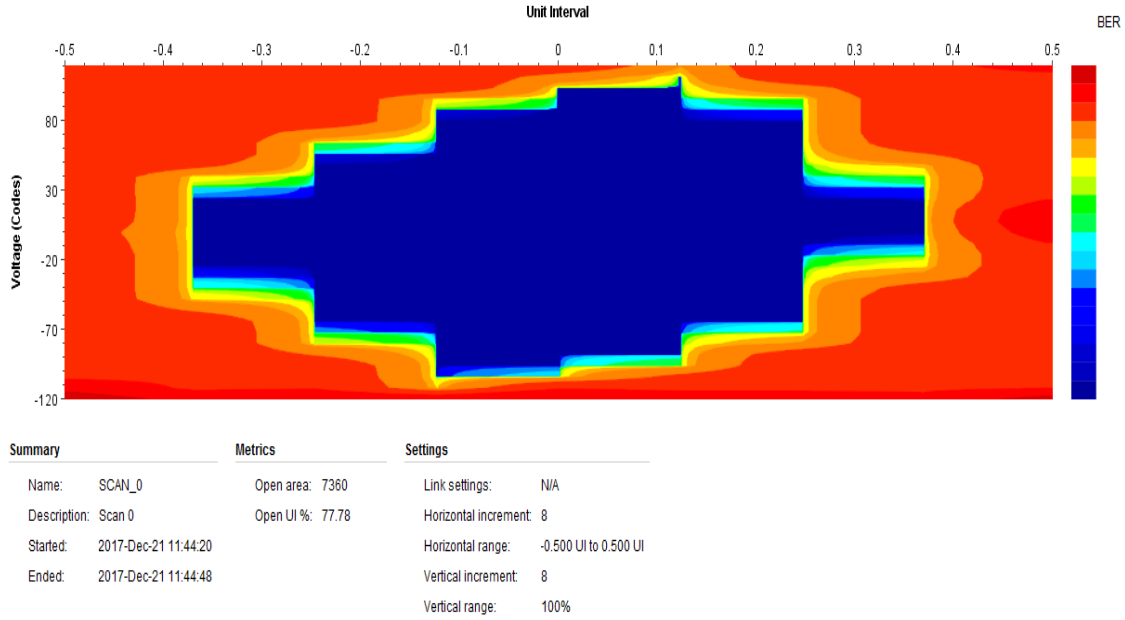


Figure 5 : EyeScan result for Link 0 of MGT Quad 213

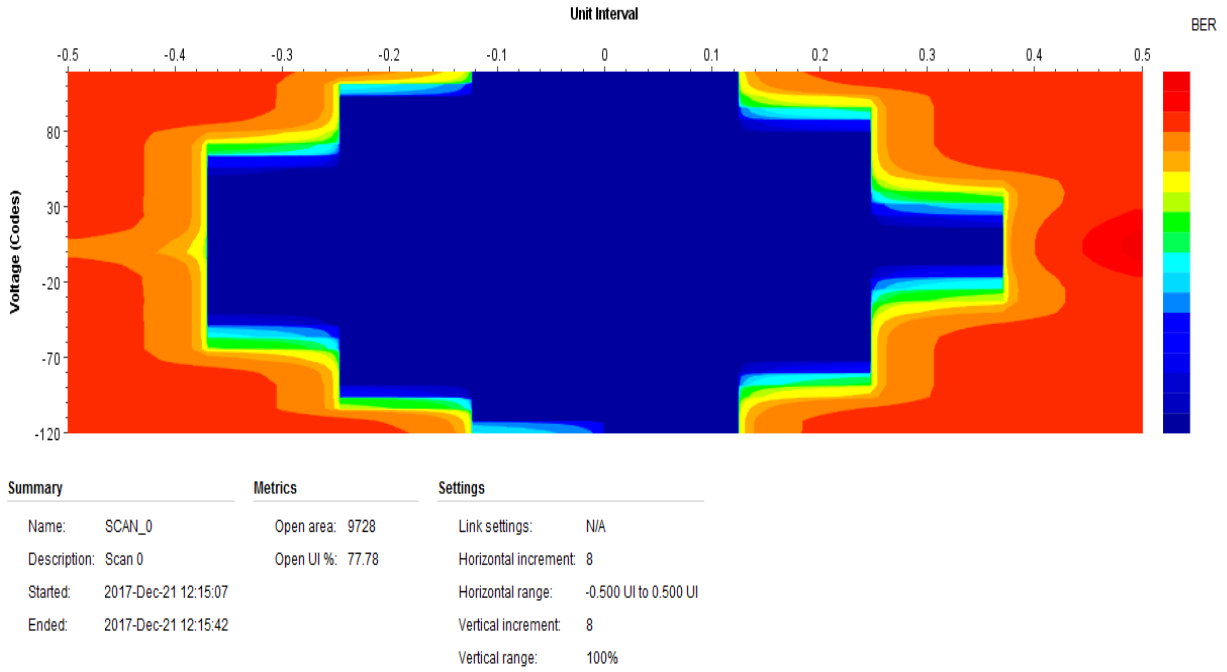


Figure 6 : EyeScan result for Link 1 of MGT Quad 213

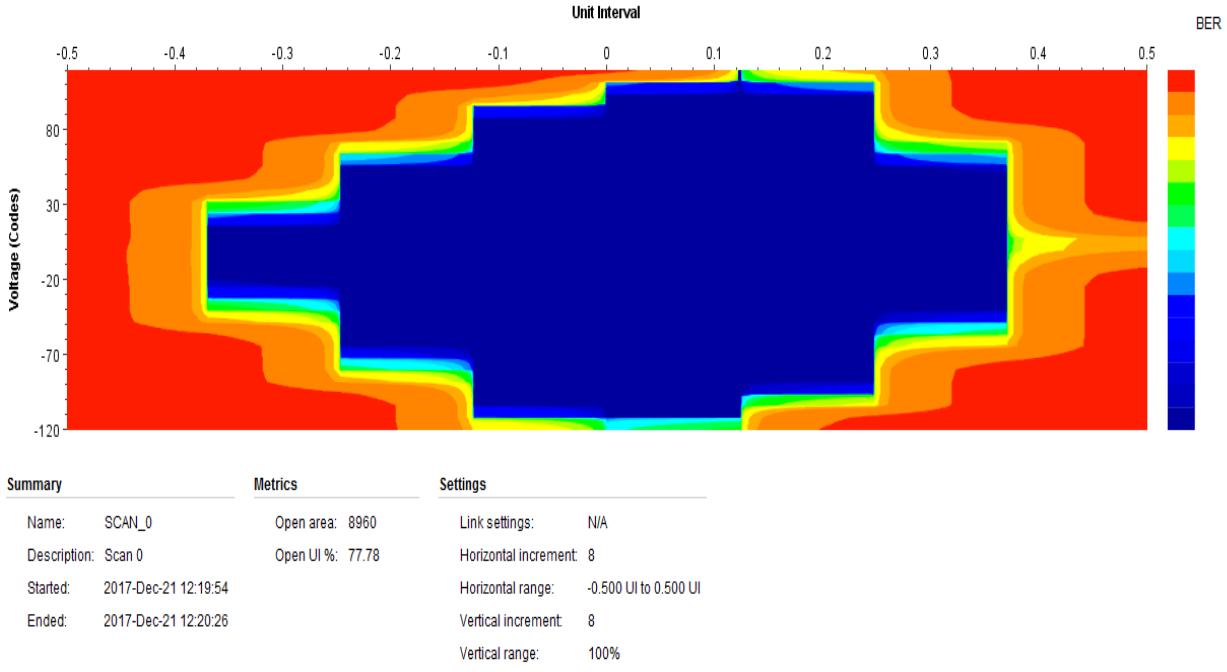


Figure 7 : EyeScan result for Link 2 of MGT Quad 213

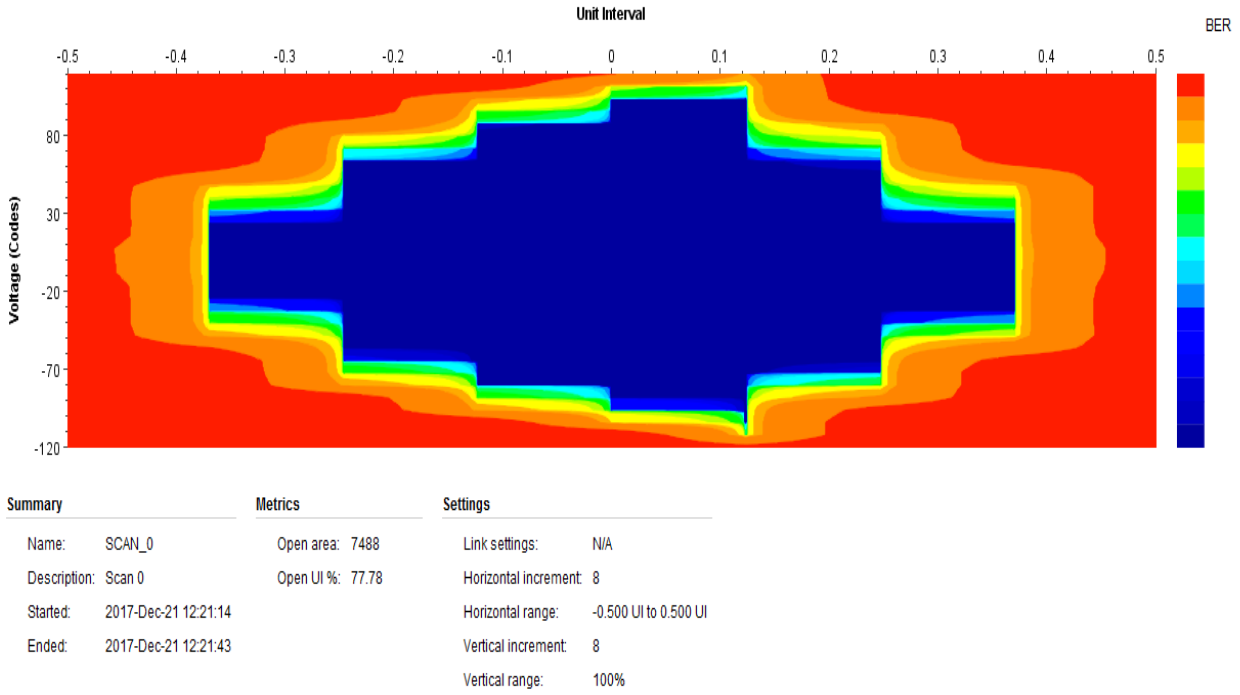


Figure 8 : EyeScan results for Link 3 of MGT Quad 213

From Figures 5, 6, 7 and 8, the Eye pattern for all the loopback channels in MGT Quad 213 can be seen to have a wide Eye opening of more than 75%. This denotes that the received signals have a high integrity and very low amplitude distortion. It also verifies that the physical medium used for loopback is hassle free and functions properly.

The GTP Quad 216 EyeScan results for all four channels are presented below. The EyeScans were performed with Slow-clock pattern being transmitted and received over the links. The links are connected in physical loopback as shown in the table.

From Figures 9, 10, 11 and 12, the Eye pattern for all the loopback channels in MGT Quad 216 can be seen to have a wide Eye opening of more than 75%. This denotes that the received signals have a high integrity and very low amplitude distortion. It also verifies that the physical medium used for loopback is hassle free and functions properly

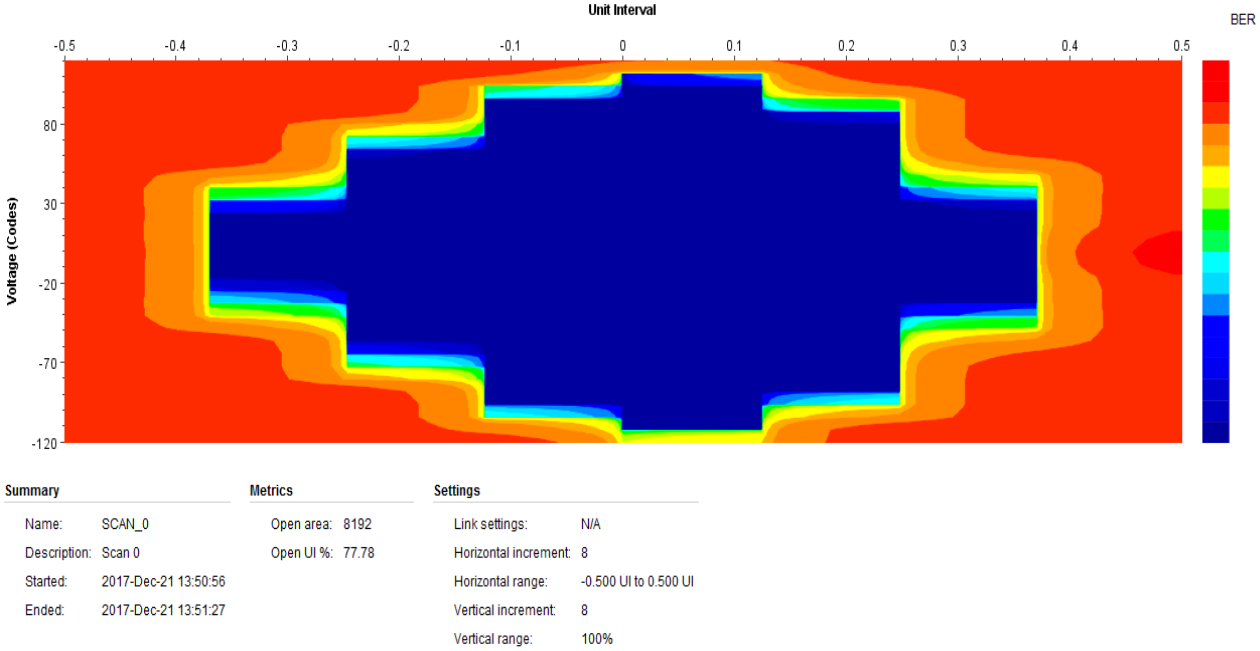


Figure 9 : EyeScan reseult for Link 0 of MGT Quad 216

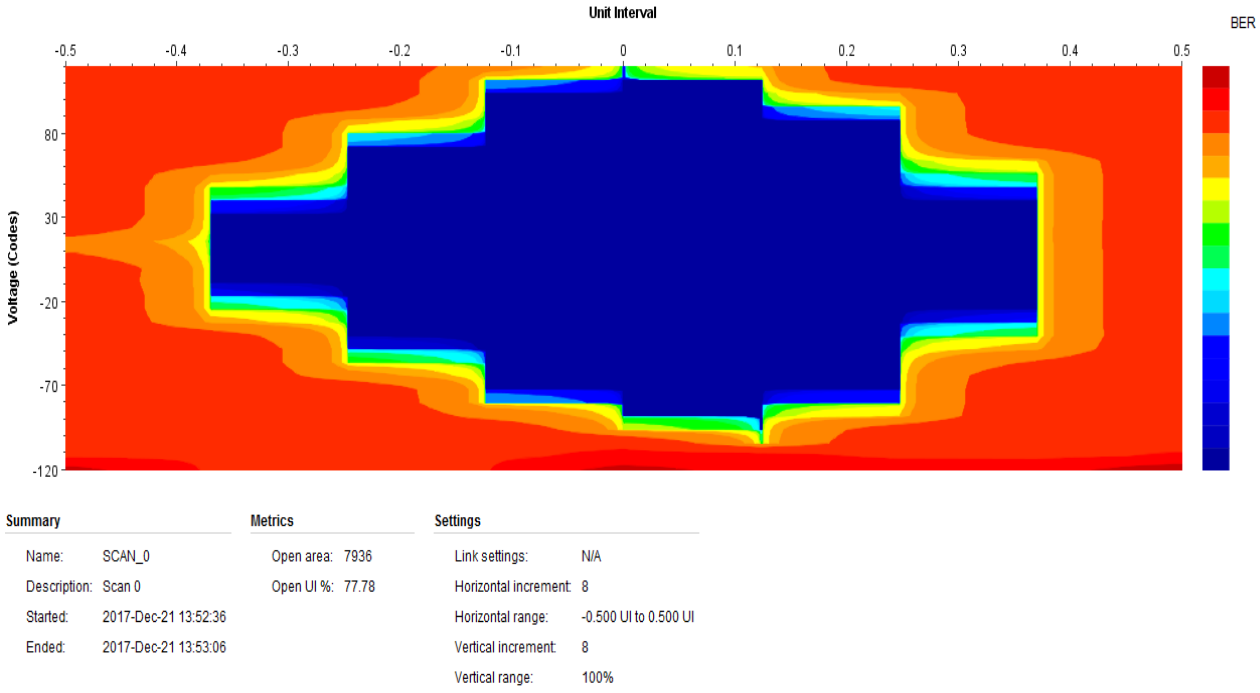


Figure 10 : EyeScan reseult for Link 1 of MGT Quad 216

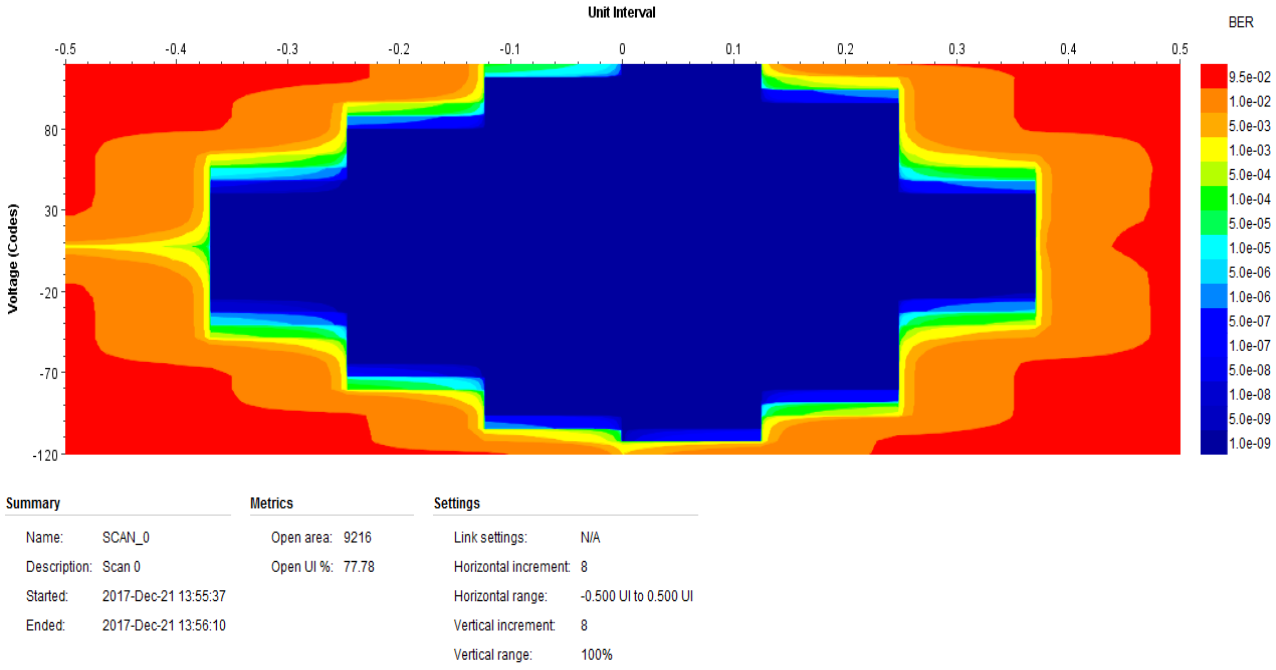


Figure 11 : EyeScan reseult for Link 2 of MGT Quad 216

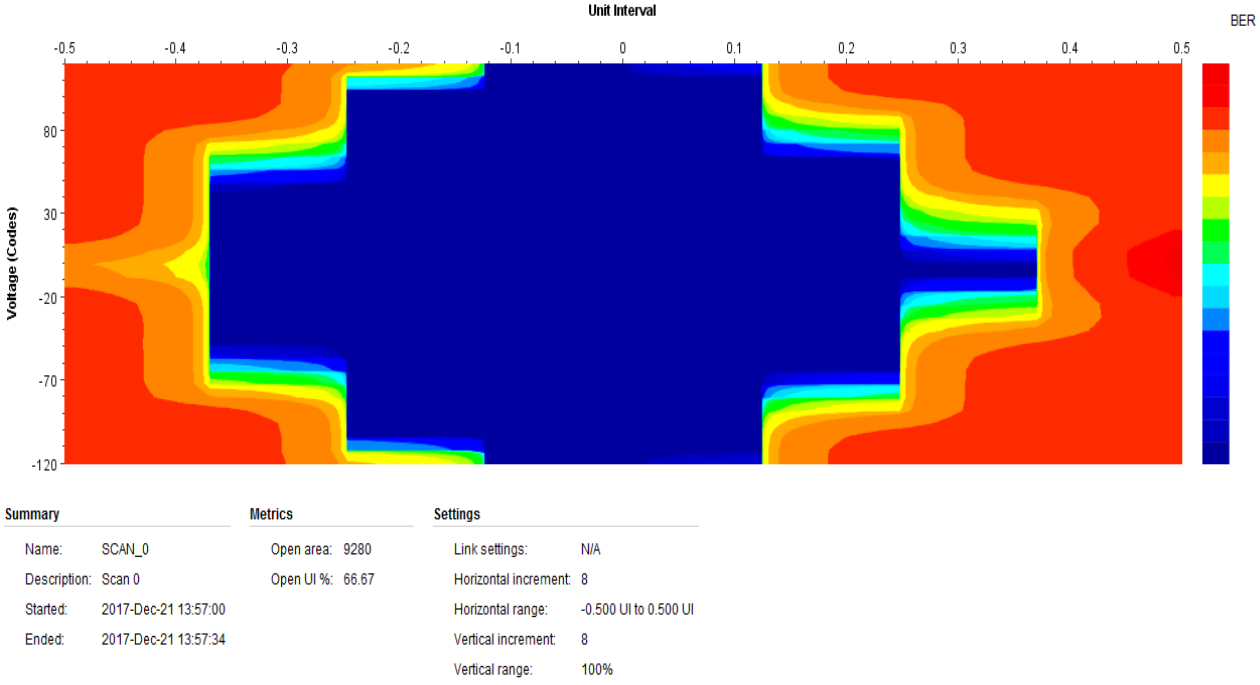


Figure 12 : EyeScan reseult for Link 3 of MGT Quad 216

Conclusion

Using the above presented Hardware Setup, tests were performed using different line rates. As discussing each of them would result in an unnecessarily long document, only the test with the fastest line rate tested is included.

After the careful analysis of each of the tests performed above, it could be safely concluded that the high-speed serial transceivers on the Artix-7 FPGA residing in the EFM-03 Beastboard are fully functional. They are capable of transferring data at at least 6.25 Gigabits per second. Also, by means of the EyeScan tests performed, it can be concluded that the physical medium used introduces very minimal noise and maintains the signal integrity.

Users can use this test as a starting point to verify the GTP functionality in a physical loopback configuration and develop their own high-speed transfer interfaces.

Revision history

Version	Date	Comment	Author	Approved by
V0.1	December, 2017	First preliminary approach	vvi	mk
v1.0	January, 2018	First Release	vvi	mk

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